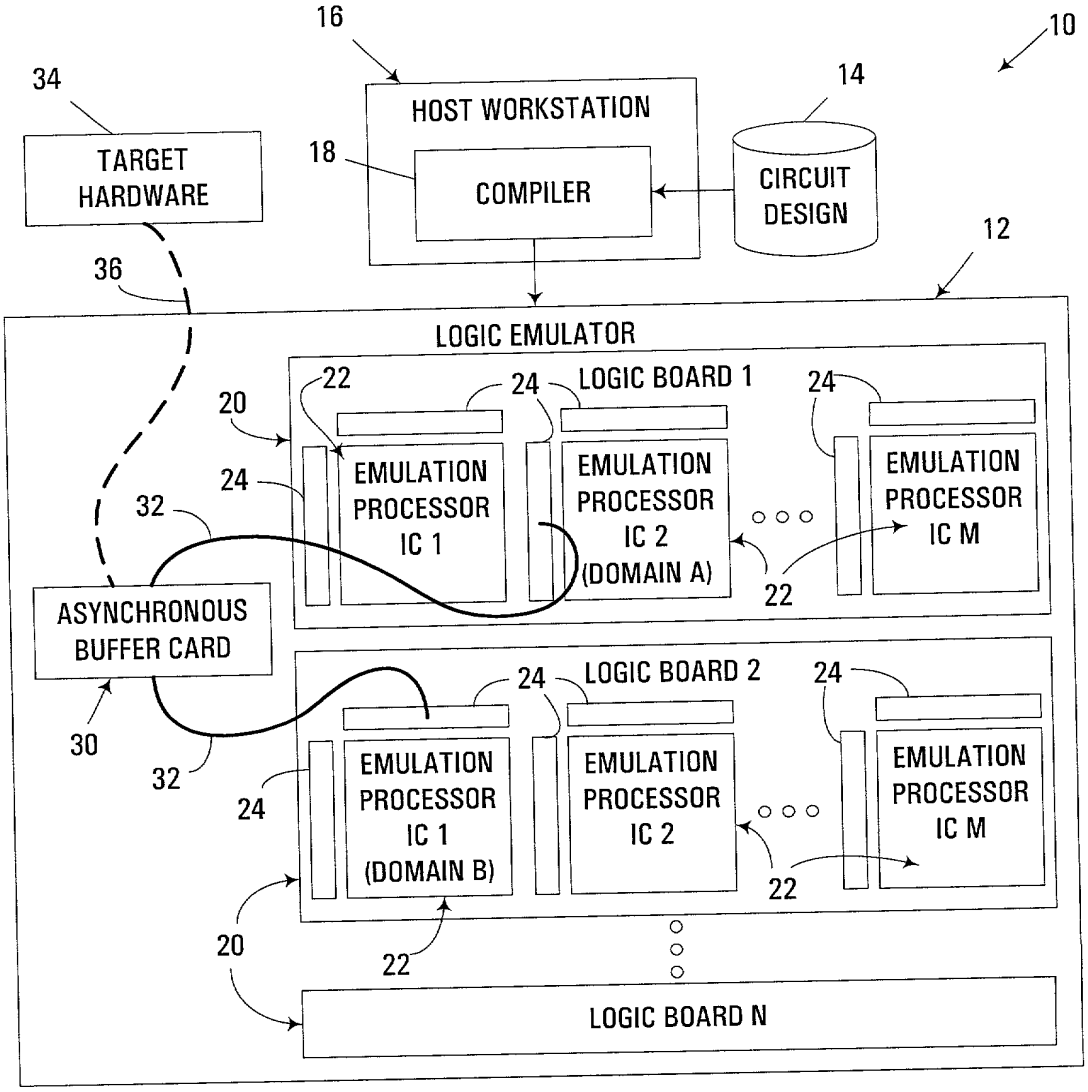
16
10
34
HOST WORKSTATION
14
TARGET HARDWARE
18
COMPILER
CIRCUIT DESIGN
12
36
LOGIC EMULATOR
22
24
LOGIC BOARD 1
20
EMULATION PROCESSOR IC 1
EMULATION PROCESSOR IC 2 (DOMAIN A)
EMULATION PROCESSOR IC M
32
ASYNCHRONOUS BUFFER CARD
LOGIC BOARD 2
30
EMULATION PROCESSOR IC 1 (DOMAIN B)
EMULATION PROCESSOR IC 2
EMULATION PROCESSOR IC M
LOGIC BOARD N

FIG. 1

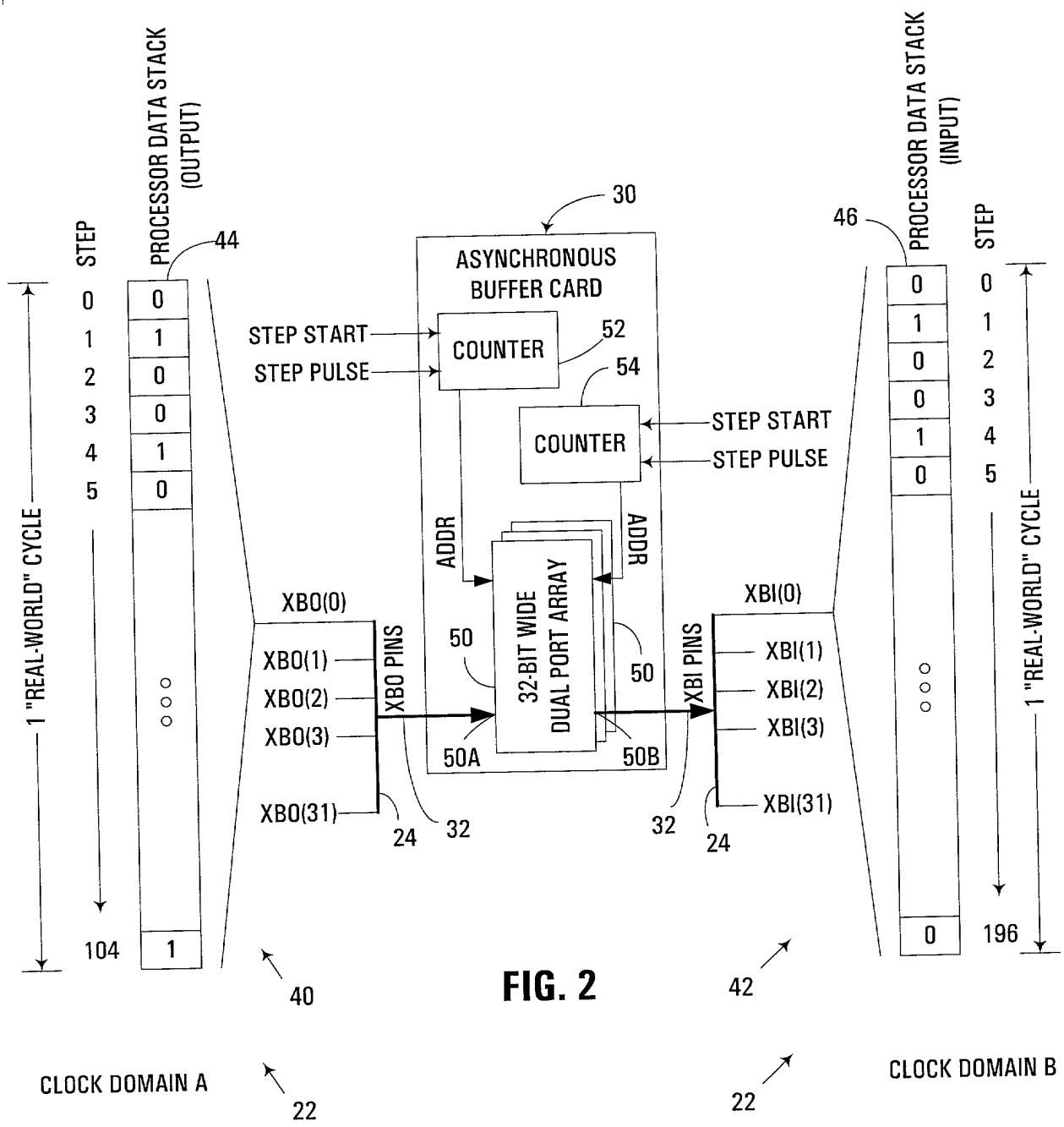
PROCESSOR DATA STACK (OUTPUT)
STEP
44
0
1
2
3
4
5
104
0
1
0
0
1
0
1
1 "REAL-WORLD" CYCLE
30
ASYNCHRONOUS BUFFER CARD
STEP START
STEP PULSE
COUNTER
52
54
COUNTER
STEP START
STEP PULSE
ADDR
ADDR
32-BIT WIDE DUAL PORT ARRAY
50
50
50A
50B
XBO(0)
XBO(1)
XBO(2)
XBO(3)
XBO(31)
XBO PINS
24
32
XBI(0)
XBI(1)
XBI(2)
XBI(3)
XBI(31)
XBI PINS
32
24
40
42
22
22
CLOCK DOMAIN A
CLOCK DOMAIN B
46
PROCESSOR DATA STACK (INPUT)
STEP
0
1
2
3
4
5
196
0
1
0
0
1
0
1 "REAL-WORLD" CYCLE

FIG. 2

TIME	CLOCK DOMAIN A			ASYNCHRONOUS BUFFER CARD									CLOCK DOMAIN B		
	STEP PULSE	STEP #	VALUE	ARRAY INPUT	CNTR A	[0]	[1]	[2]	[3]	[4]	[5]	CNTR B	ARRAY OUTPUT	STEP PULSE	STEP #	VALUE READ
0				X	X	X	X	X	X	X	X	X	X			
1	ACTIVE	0	X	X	RESET 0	X	X	X	X	X	X	X	X			
2	ACTIVE	1	BUSB(9)=1	1	1	X	1	X	X	X	X	X	X			
3	ACTIVE	2	ENABLE=0	0	2	X	1	0	X	X	X	RESET 0	X	ACTIVE	0	X
4	ACTIVE	3	FLUSH=0	0	3	X	1	0	0	X	X	1	1	ACTIVE	1	BUSB(9)=1
5	ACTIVE	4	X	X	4	X	1	0	0	X	X	2	0	ACTIVE	2	ENABLE=0
6	ACTIVE	5	X	X	5	X	1	0	0	X	X	3	0	ACTIVE	3	FLUSH=0
7				X	5	X	1	0	0	X	X	3	0			
8				X	5	X	1	0	0	X	X	3	0			
9				X	5	X	1	0	0	X	X	3	0			
10				X	5	X	1	0	0	X	X	RESET 0	X	ACTIVE	0	X
11				X	5	X	1	0	0	X	X	1	1	ACTIVE	1	BUSB(9)=1
12				X	5	X	1	0	0	X	X	2	0	ACTIVE	2	ENABLE=0
13				X	5	X	1	0	0	X	X	3	0	ACTIVE	3	FLUSH=0
14				X	5	X	1	0	0	X	X	3	0			
15	ACTIVE	0	X	X	RESET 0	X	1	0	0	X	X	3	0			
16	ACTIVE	1	BUSB(9)=0	0	1	X	0	0	0	X	X	RESET 0	X	ACTIVE	0	X
17	ACTIVE	2	ENABLE=1	1	2	X	0	1	0	X	X	1	0	ACTIVE	1	BUSB(9)=0
18	ACTIVE	3	FLUSH=0	0	3	X	0	1	0	X	X	2	1	ACTIVE	2	ENABLE=1
19	ACTIVE	4	X	X	4	X	0	1	0	X	X	3	0	ACTIVE	3	FLUSH=0
20	ACTIVE	5	X	X	5	X	0	1	0	X	X	3	0			
21				X	5	X	0	1	0	X	X	3	0			
22	ACTIVE	0	X	X	RESET 0	X	0	1	0	X	X	3	0			
23	ACTIVE	1	BUSB(9)=0	0	1	X	0	1	0	X	X	3	0			
24	ACTIVE	2	ENABLE=1	1	2	X	0	1	0	X	X	3	0			
25	ACTIVE	3	FLUSH=1	1	3	X	0	1	1	X	X	3	0			
26	ACTIVE	4	X	X	4	X	0	1	1	X	X	3	0			
27	ACTIVE	5	X	X	5	X	0	1	1	X	X	3	0			
28				X	5	X	0	1	1	X	X	3	0			
29	ACTIVE	0	X	X	RESET 0	X	0	1	1	X	X	RESET 0	X	ACTIVE	0	X
30	ACTIVE	1	BUSB(9)=1	1	1	X	1	1	1	X	X	1	X (Unstable)	ACTIVE	1	BUSB(9)=X
31	ACTIVE	2	ENABLE=0	0	2	X	1	0	1	X	X	2	X (Unstable)	ACTIVE	2	ENABLE=X
32	ACTIVE	3	FLUSH=0	0	3	X	1	0	0	X	X	3	X (Unstable)	ACTIVE	3	FLUSH=X
33	ACTIVE	4	X	X	4	X	1	0	0	X	X	3	X			
34	ACTIVE	5	X	X	5	X	1	0	0	X	X	RESET 0	X	ACTIVE	0	X
35				X	5	X	1	0	0	X	X	1	0	ACTIVE	1	BUSB(9)=1
36				X	5	X	1	0	0	X	X	2	1	ACTIVE	2	ENABLE=0
37				X	5	X	1	0	0	X	X	3	1	ACTIVE	3	FLUSH=0
38				X	5	X	1	0	0	X	X	3	1			

FIG. 3